REMARKS

Applicants acknowledge receipt of the Examiner's Office Action dated February 4, 2005. This Office Action rejects all pending claims. The rejection was made final. In light of the foregoing amendments and following remarks, Applicants respectfully request the Examiner's reconsideration and reexamination of all pending claims.

Claims 19 – 32 are pending in this application. The February 4, 2005, Office Action rejects claims 19 and 25 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,449,732 issued to Rasmussen et al. ("Rasmussen"). Claims 20 and 31 stand rejected under 35 U.S.C. § 103 as being unpatentable over Rasmussen in view of U.S. Patent No. 6,003,130 issued to Anderson ("Anderson"). Claims 21 – 24 and 32 stand rejected under 35 U.S.C. § 103 as being unpatentable over Rasmussen in view of Anderson as applied to claims 20 and 31 in the February 4, 2005, Office Action, and further in view of U.S. Patent No. 5,878,248 issued to Tehranian et al. ("Tehranian"). Lastly, claims 26 – 30 stand rejected under 35 U.S.C. § 103 as being unpatentable over Anderson in view of Rasmussen.

The rejections set forth in the February 4, 2005, Office Action mirror rejections contained in the June 7, 2004, Office Action. Applicants addressed the rejections of the June 7, 2004, Office Action in their response filed on September 7, 2004. This response incorporates the arguments made in the September 7, 2004 response.

In addition to mirroring the specific rejections in the June 7, 2004, Office Action, the February 4, 2005, Office Action addresses arguments made by Applicants in their response filed September 7, 2004. Specifically, the Final Office Action states:

> In response to the Applicants' arguments that "the cited section within Rasmussen does not indicate that the development port of the processor module is coupled to a bus formed on a print circuit board," and that the reference does "not state that an optional port is coupled to a bus formed on a printed circuit board," the arguments have been fully considered but are not deemed persuasive, because Rasmussen et al. teaches the above as shown in Fig. 10B, as well as in column 13, lines 12-25.

Applicants have reviewed Fig. 10B and column 13, lines 12-25 in Rasmussen and can find no teaching or fair suggestion of a processor development port which is coupled to a bus formed on a printed circuit board or an optional port coupled to a bus formed on a printed circuit board. Specifically, column 13, lines 12 – 25 of Rasmussen set forth:

> With reference to FIG. **10**B, an alternate configuration of the triplicated main processors **1***a*, **1***b* and **1***c* is shown utilizing dual communication modules **3***a* and **3***b* which provide Modbus and Development serial links, but in addition provide external communication links for external communications. In this configuration the Modbus **5** and Development **6** ports on the MP/IOP modules **1***a*, **1***b*, and **1***c* are disabled. Each of the LCM modules **3**a and **3**b communicates with each of the respective MP/IOP modules **1** over communication lines **9***a*, **9***b* and **9***c* which are coupled to the communication bus (LCB) of each of the main processors. FIG. **10**B also shows additional LIO modules **2***c* and **2***d* attached to the LIO bus to illustrate that multiple LIO modules **2** may be connected on the same LIO bus **13**.

The inconsistency in Figure 10B and the text of column 13, lines 12 – 25 is ntoed and presents an issue of enablement. For example, column 13, lines 12 – 25 uses reference numbers 1a, 1b, and 1c to identify main processors and MP/IOP modules. Column 13, lines 12 – 25 also states that main processors 1a, 1b, and 1c utilize dual

communication modules 3a and 3b. However, communication modules 3a and 3b are not shown in Figure 10B. Column 13, lines 12 – 25 discloses communication lines 9a, 9b, and 9c and LIO modules 2c and 2d, but these elements are not disclosed in Figure 10B. These inconsistencies and others in column 13, lines 12 – 25 of Rasmussen render column 13, lines 12 – 25 non-enabling. Non-enabling art cannot be used to reject claims under 35 USC § 102.

Notwithstanding the non-enabling aspects of Rasmussen, column 13, lines 12 – 25 of Rasmussen does not teach or fairly suggest a second bus formed on the first printed circuit board and coupled to the development port of a processor as required by independent claim 19. The aforementioned paragraph does teach "Development 6 ports" on MP/IOP modules 1a, 1b, and 1c, but column 13, lines 12 – 25 fails to teach or fairly suggest "Development 6 ports" are coupled to a second bus formed on a printed circuit board. Indeed, column 13, lines 12 – 25 implies that "Development 6 ports" are not coupled at all since column 13, line 20 states that Development 6 ports "are disabled."

Clearly, nothing in the aforementioned paragraph sets forth that a second bus is formed on a first printed circuit board and is coupled to the development port of a processor. At best, the aforementioned paragraph in Rasmussen is inconclusive in teaching this limitation of independent claim 19. It is through the development port coupled to the second bus formed on the first printed circuit board that boot up code is transmitted to the processor of the first printed circuit board as required in dependent claim 20. Accordingly, Applicants submit that independent claim 19 is patentably distinguishable over Rasmussen.

The Final Office Action also states:

> In response to the applicant's arguments that nothing would indicate "that a development PC communicates with the processor module of Rasmussen via a bus which is mounted on a printed circuit board which in turn is coupled to a development port of a processor module which is also mounted on the printed circuit board," the arguments have been fully considered but are not deemed persuasive, because Rasmussen et al. teaches a development port (column 4, lines 59 – 66), mounted on a printed circuit board (column 5, lines 13 – 17), with a system bus coupled to the processor (column 2, lines 21 – 67).

Column 4, lines 59 – 66 discloses that each processor module contains two ports that could be used for interface for the development computer system or as a slave interface. Further, this cited section of Rasmussen teaches that each processor module also contains one optional port for system executive development or at LANS support.

Column 5, lines 13–17 sets forth:

> As each input/output module is scanned, the new input data is transmitted by the input/output module to processor module via shared memory located on the printed circuit board supporting the processor module and the input/output module.

This cited section sets forth that a printed circuit board supports a processor module.

Column 2, lines 21–67 sets forth:

> The system is a scan based system and once per scan, the MP module synchronizes and communicate with the neighboring MP's over the Channel 11. The Channel 11 forwards copies of all analog and digital input data to each MP, and compares output data from each MP. The MPs vote the input data, execute the application program and send outputs generated by the application program to the output modules. In addition, the controller votes the output data on the output modules as close to the field as possible to detect and compensate for any errors that could occur between the Channel 11 voting and the final output driven to the field. For each I/O module, the controller can support an option hot-spare module. If present, the hot-spare takes control if a fault is detected on the primary module during operation. The hot-spare position is also used for the online-hot repair of a faulty I/O module.
>
> The MP modules each control a separate channel and operates in parallel with the other two MPs. A dedicated I/O control processor on each MP manages the data exchanged between the MP and the I/O modules. A triplicated I/O bus, located on the base plates, extends from one column of I/O modules to another column of I/O modules using I/O bus cables. In this way the system can be expanded. Each MP poles the appropriate channel of the I/O bus and the I/O bus transmits new input data to the MP on the polling channel. The input data is assembled into a table in the MP and is stored in memory for use in the voting process.
>
> Each input table in each MP is transferred to its neighboring MP over the Channel 11. After this transfer, voting takes place. The Channel 11 uses a programmable device with a direct memory access to synchronize, transmit, and compare data among the three MPs.
> If a disagreement occurs, the signal value fount in two of three tables prevails, and the third table is

> corrected accordingly. Each MP maintains data about necessary correction in local memory. Any disparity is flagged and used at the end of the scan by built-in fault analyzer routines to determine whether a fault exists on a particular module.
>
> The MPs send corrected data to the application program and then executes the application program in parallel with the neighboring MP and generates a table of output values that are based on the table of input values according to user-defined rules. The I/O control processor on each MP manages the transmission of output data to the output modules by means of the I/O bus.

This cited section teaches a high speed bus (channel 11) coupled to main processor modules (MP). Even though (1) column 4, lines 59–66 may teach a development port, (2) column 5, lines 13–17 may teach a processor supported on a printed circuit board, and (3) column 2, lines 21–67 may teach a bus coupled to a processor, these cited sections of Rasmussen fail to teach or fairly suggest that the development port of column 4, lines 59–66 are contained within the processor supported by the printed circuit board in column 5, lines 13–17, or that the development port set forth in column 4, lines 59– 66 is coupled to channel 11 set forth in column 2, lines 21 –67, or that channel 11 is mounted to the same circuit board that supports the processor in column 5, lines 13–17. Lastly, applicants reserve the right to contest the office action's basis for combining the cited references to reject claims under 35 USC Section 103.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5093.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Mail Stop AF, COMMISSIONER FOR PATENTS, P. O. Box 1450, Alexandria, VA 22313-1450, on March 28, 2005.

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